FPGA BASED SYSTEM DESIGN

QUIZ NO 02

NAME: ROLL NO:

SEMMESTER VIII DATE: 13TH MAR, 2014

1. Casex does support? . True / False (1)
2. Case does support? . True / False (1)
3. What are the differences between VERILOG and VHDL.(3)
4. Declared modules cannot be instantiated. True / False (1)
5. INOUT is a reserve word. True / False (1)
6. Initial command is terminated with a reserve key word end. True / False (1)
7. What is the length of integers? (1)
8. Integers are recommended for synthesis. True / False (1)
9. Sequence of non-blocking assignments executes sequentially. True / False (1)
10. Find the error in the following code and correct the code as well. (9)
11. @module mux2to1 (y,a,b,sel);

output y;

inputa,b :

reg y [n-1:0]:

inputsel;

always @ (a | b or sel)

if(sel)

y = a;

else,

y = b;

endmodule

1. module sum@ur code(sum,datain,clk)”

output sum?

Input data\_in, clk;

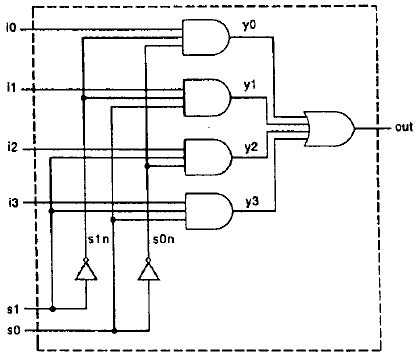
reg I;

always @ (pos\_edgeclk)

for (I = 0, I < 5; I = i+1)

sum = sum + datain[i];

endmodule



Q1. Draw the schematic of complementary Nand Gate.

Q2. Draw the schematic of complementary of Nor Gate.